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A STUDY ON PROTOTYPE DRIVE - CONSTRUCTION AND CONTROL IMPLEMENTATION

Ganesh Pashikanti, Research Scholar under the faculty of Electrical Engineering at SSSUTMS, Sehore.
Dr. A A Ansari Associate Professor -ECE/EE, SSSUTMS-Sehore
Dr.N.Bhoopal (Professor & HOD) BVRIT(A), Narsapur,Medak,Telangana

ABSTRACT

The paper includes construction and control implementation of prototype drive, FPGA, and FPGA controller design. Two control procedures have been proposed to be specific the single band, and novel double band strategies, and thought has been given to the most fitting manner by which to execute the control. The result of this is that a FPGA is the supported stage due to the solid, unsurprising manner by which they work, and the reasonableness of such a chip for execution of the rationale based control plans.

KEYWORDS: control, prototype, design, band, single, matrix.

I. INTRODUCTION

The Prototype Single Sided Matrix Converter was planned in a measured form, considering simple extension of phase numbers. A block graph indicating the structure of the 3-phase SSMC and controller can be found in figure 1, while figure 2 shows a photo of the total 4-phase SSMC. More Photos can be found in index E. The control of the SSMC is performed by the FPGA card. It gets input voltage and output current information by means of its on-board simple to computerized converters, and cycles this information utilizing a custom FPGA program. The input voltage signals are providedby a voltage estimation PCB, while the output current estimations come legitimately from the output phase power circuit PCB's. The FPGA controller program produces the door signals for the IGBT's which make up the matrix converter power circuit. These signals are gotten from the input voltage and output current information. The entryway drive signals created by this program are then fed through a short lead

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to a current mirrors PCB. This board takes the door drive signals in advanced voltage form, and converts them to currents, to be fed to the matrix converter entryway drive circuits. There is then

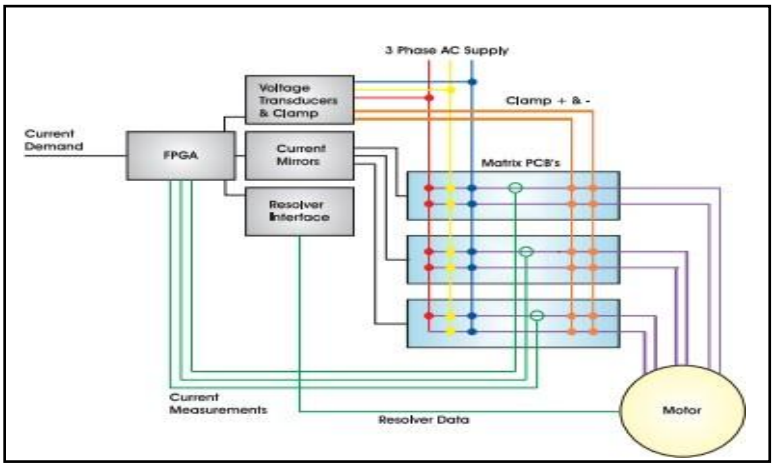
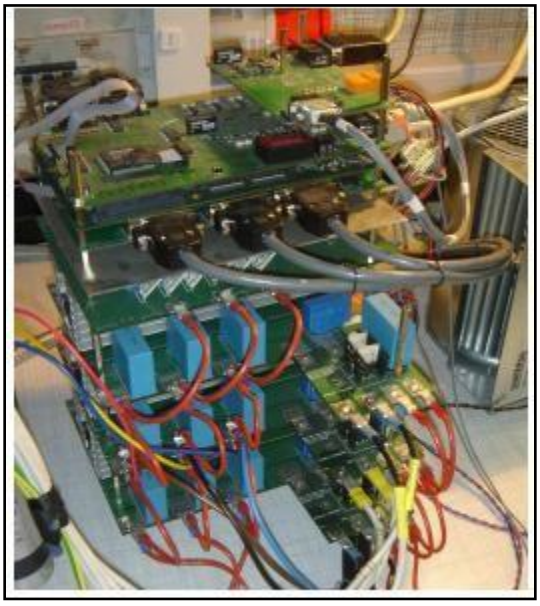


Figure 1: Block Diagram Showing the Structure of the 3-Phase SSMC



(a)

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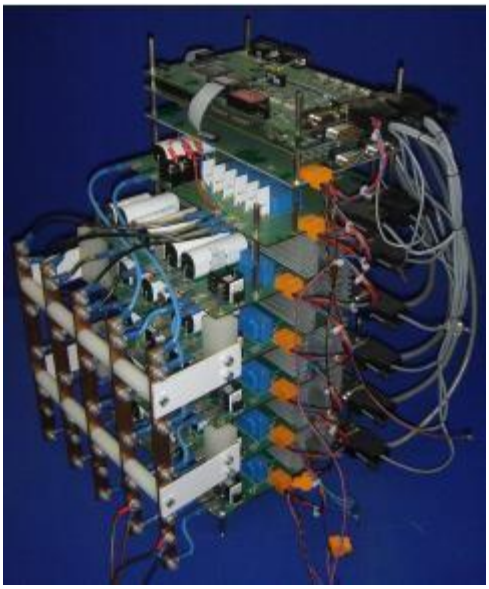

(b)

Figure 2: Single Sided Matrix Converters. a,3-Phase. b,4-Phase

II. CONVERTER HARDWARE

FPGA Controller PCB

The FPGA card used to control the SSMC was initially planned by Lee Empringham from the PEMC gathering of Nottingham University for the TIMES venture. The TIMES venture required a controller for a conventional Matrix Converter. A Texas Instrument C6711 coasting point DSP and the DSP Starter Kit (DSK) were utilized, and joined with the created FPGA card to give full control and dependable operation of a conventional matrix converter. While satisfying this job successfully, the FPGA card has end up being an entirely adaptable and flexible card in numerous different applications. In this application, a totally new program was produced for the FPGA, permitting the SSMC to be controlled without the requirement for a DSP (despite the fact that the interface with the DSP was as yet utilized while building up the FPGA program, and as information catch utility). The FPGA chip utilized is an Actel A400k ProAsic gadget.

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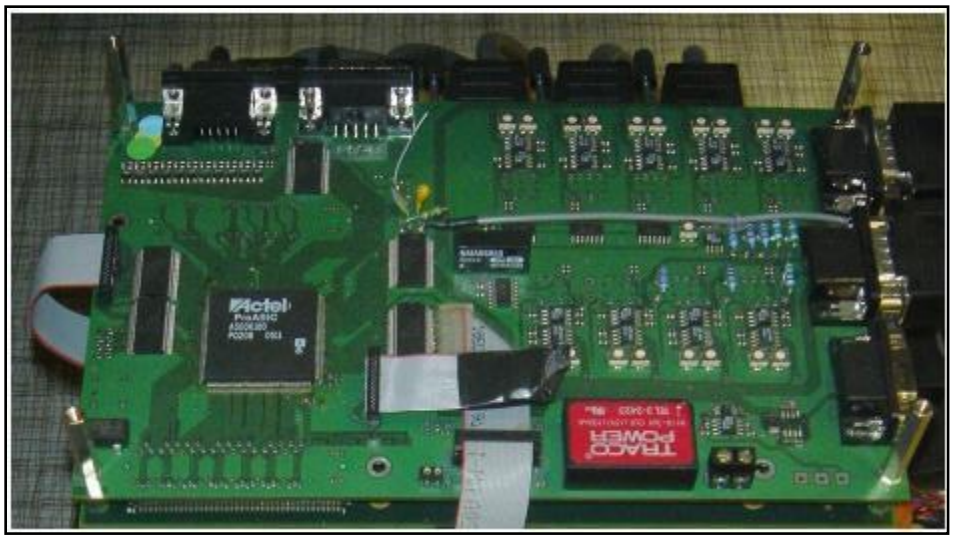

Figure 3: FPGA Controller PCB.

Resolver Interface PCB

Rotor position data is acquired using a resolver, mounted on the rotor shaft. A pair of IC chips are used with the resolver, and mounted on the resolver interface PCB. This can be seen in figure 4.

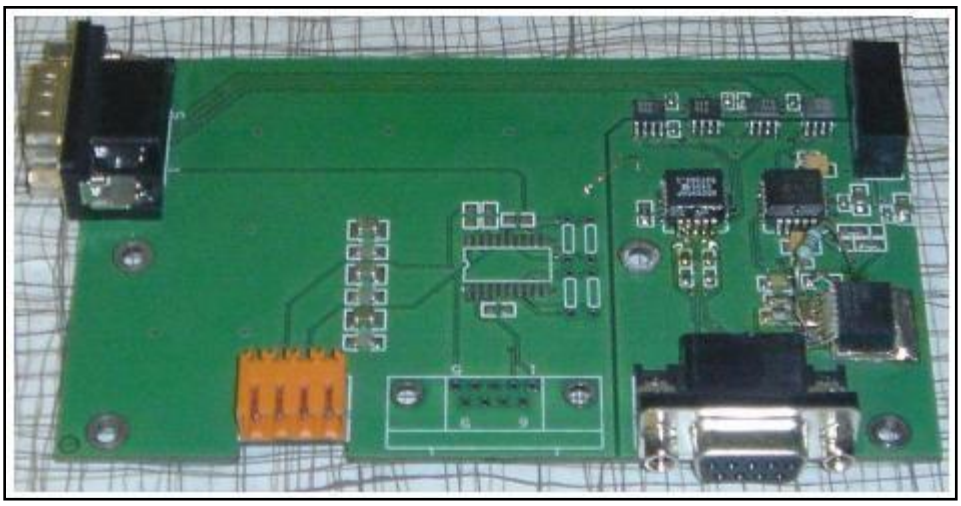

Figure 4: Resolver Interface PCB.

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Current Mirrors PCB

The current mirrors PCB is utilized to create current signals dependent on the door drive signals. These are provided in voltage form by the FPGA, through cradle chips. The current mirrors PCB can be found in figure 5 as matrix converters produce a lot of high frequency electro-magnetic noise, guarantee that operation basic signals, for example, the entryway drive signals were exceptionally noise safe. The door drive signals must be moved from the controller card, down to each of the matrix power PCB's, which in this application were arranged in a vertical pinnacle with the controller card at the top. The most noise resistant approach to move such digital signals is utilize optical strands, with transmitters and collectors for each entryway signal. Anyway the optical transmitters and collectors are expensive, so for this prototype the signals were moved as currents. To add to the noise insusceptibility of the signals, they were sent utilizing turned pair, protected links.

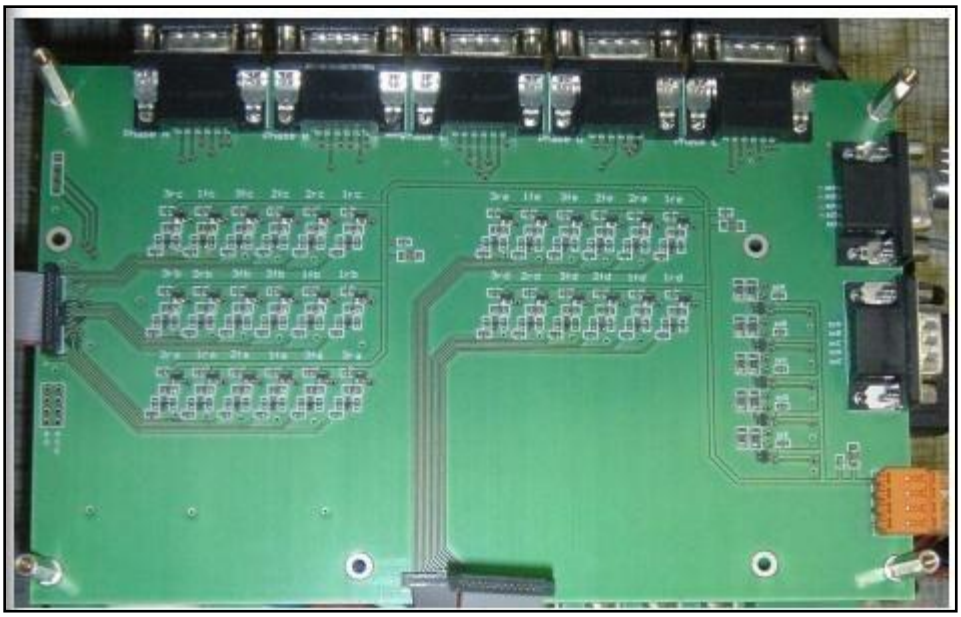

Figure 5: Current Mirrors PCB.

Voltage Transducers and Clamp PCB

The operation of the SSMC requires estimation of the input voltages. As this prototype SSMC was planned in an expandable form, with a different matrix PCB for each output phase, it was logical to house the input voltage transducers and input voltage cinch on a different PCB. This is appeared in figure 6. The

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voltages estimated are the three line to line voltages. It would have been conceivable to gauge only two of the line to line voltages, and recreate the third, anyway this would have presented extra computational demands, and might not have been accurate, particularly if huge twisting and awkwardness were available, or incited on the voltage supply.

Figure 6: Voltage Transducers and Clamp PCB.

III. FPGA CONTROLLER DESIGN

A FPGA was utilized to control the SSMC. This screens the input voltages and output currents of the matrix converter, and utilizing the control calculation actualized within the FPGA program, figures out which switches of the matrix converter should be activated so as to control the output current at the necessary level. The program utilized in the FPGA was grown explicitly for this venture, and actualized both the single band and double band hysteretic control methods. Actel's Libero advancement suite was utilized to create the program. The FPGA program is composed utilizing the VHDL programming language. The code for this might be input legitimately, or then again the 'ViewDraw' program included with Libero might be utilized to generate the VHDL. The ViewDraw program is generated graphically, utilizing blocks to speak to specific capacities. A large number of these blocks are generated utilizing macros, created by a further component of Libero, 'SmartGen', which generates adjustable blocks, for example, logic gates, registers and counters. Different blocks can be created to speak to VHDL code input straightforwardly by the developer. The SSMC control program was created thusly, utilizing a blend of programming methods. The VHDL code for the final controller program, which had the option to execute both the single and double

band control strategies, was more than 220,000 lines This demonstrates the value of such a graphical, halfway mechanized programming strategy, as entering such a length of code physically would be both tedious, and its operation would be inherently hard to picture. All through the program improvement, simulations are performed utilizing 'ModelSim'. An improvement document is generated for a specific block, utilizing 'WaveFormer'.

FPGA Design Considerations

While delivering a FPGA program, one must recall that the final product is a synchronous logic circuit format. This makes the programming procedure to some degree distinctive to creating a program for either a PC or a Digital Signal Processor (DSP). The main factor to shoulder at the top of the priority list is that the software engineer is answerable for guaranteeing the legitimacy of information at each progression of the synchronous program.

- **Data Validity:** All numbers handled by the FPGA are spoken to in paired form. This infers that various 'lines' are utilized for each number. There is no committed directing asset within the FPGA chip, so these lines may take any accessible way through the FPGA between operational blocks. Despite the fact that Libero endeavors to limit propagation postpones all things considered, these ways will have differing propagation times. Likewise, operations on one line may take longer than operations on a second. Consequently, registers are utilized between operations, guaranteeing that a total set of legitimate data is available at the input to the register, prior to being clocked through to the following operation, by the framework clock.

- **Numerical Manipulation:** Another extremely huge ramification of creating a FPGA program is that the mathematical control capabilities of the FPGA are restricted. Smartgen can be utilized to deliver Adders, Subtractors and Multipliers, which reach the final value within a single clock cycle. Division on the FPGA is anyway an undeniably more mind boggling and tedious operation, and there is no SmartGen macro accessible for delivering such an administrator. Division by any whole number is conceivable, and a method was executed during the advancement of the SSMC controller, however depends on an iterative method. The quantity of clock

cycles needed by the method tried was the quantity of bits of the input values, in addition to one. This is plainly not ideal for the extremely high bandwidth control loops, and division by such numbers was hence stayed away from. The elective approach to performing actual division is bit-moving. By moving the characters of the parallel portrayal of a number 'n' position to the right, the number is partitioned by 2^n. This is an exceptionally effective method for performing division, anyway the denominator has a predetermined number of values ie. 2^n. where division by a constant is required, a mix of an augmentation, trailed by a bit-move can be utilized. This permits division by any whole number in only two clock cycles. A blend of augmentation by an enormous non 2^n number, trailed by a huge bit-move to lessen the number back within its original range likewise took into account duplication by little scaling factors with various decimal places. This was vital while rectifying the values estimated by the A/D converter chips, as the transducers utilized had a huge offset related with them. Plainly the resolution of the number is diminished as the value is moved back down, as the most un-critical bits are lost, anyway this didn't cause a problem.

- **State Machines:** A state machine is a gadget where the output is an element of both the prompt inputs to the framework, and a past state. The operation of a state machine might be shown as either a state diagram or state table. Table 1 and figure 7 show a state table and state diagram individually for a similar model framework. So as to guarantee that the past state data is legitimate, registers are utilized at the input, clocking the data into the state machine at a fixed frequency. This applies to all inputs to that state machine, not simply the past state data. Components of the control operation for both the single band and double band control methods for the SSMC were spoken to utilizing truth tables when first characterizing the operation of the control strategy, and while mimicking the controller utilizing the Simulink component of Matlab. From these 'truth', or 'state' tables, it was conceivable to generate VHDL code for the state machine, to be input legitimately into Libero.

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Table 1: Typical State Table

Present State		**Input**	**Next State**		**Output**
Q1	Q2	X	A	B	Y
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	0	1

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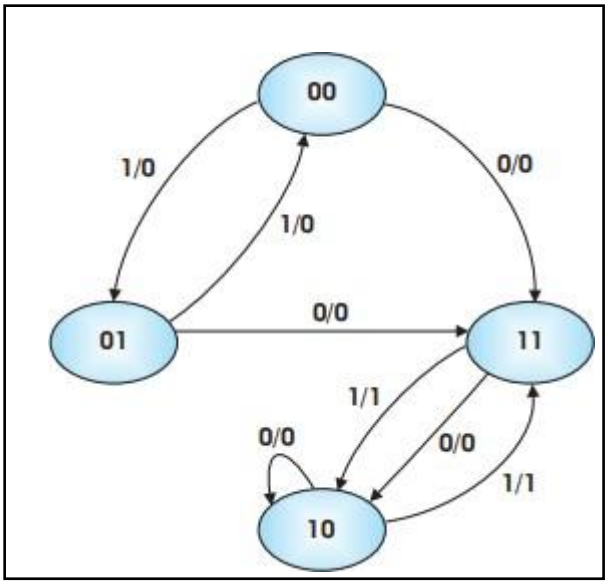

Figure 7: Typical State Diagram

IV. CONTROL STRUCTURE FOR FPGA

An outline of the control structure for the SSMC can be found in figure 8, A clarification of the operation of the FPGA program is then given in the accompanying areas, alongside graphical portrayals of the program finishing one way down the pecking order of program blocks within the phase current controller, finally reaching a segment of VHDL code speaking to a Mealy State Machine.

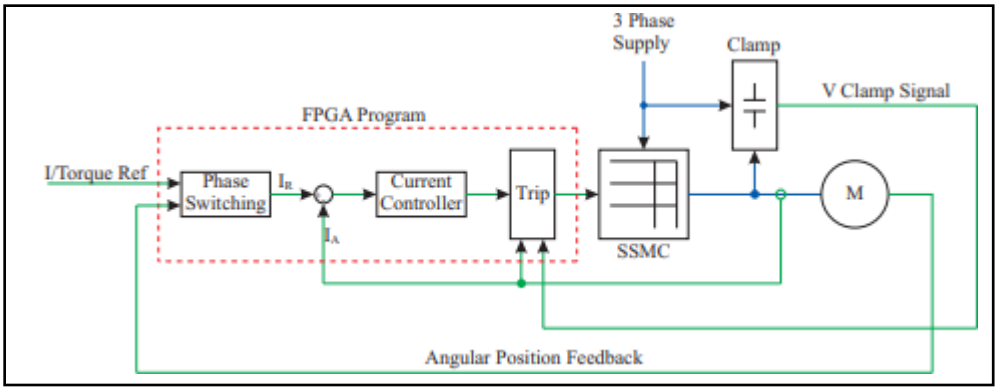

Figure 8: Control Structure.

V. CONCLUSION

This postulation has introduced the practical usage of the Single Sided Matrix Converter; utilizing control gave by a FPGA. The converter equipment has been portrayed, including the design of a six layer PCB used to give the power planes important to dependable operation of the matrix converter. The design methodology and methods utilized for execution of the drive controller within the FPGA were then introduced, followed by a depiction of the two current control conspire blocks. Excursions were incorporated within the controller to such an extent that the drive was secured under fault conditions, lastly a depiction of the DSP and Host interface were given, which in spite of the fact that not needed for the controller operation, were significant as program improvement tools.

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